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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,765	11/19/2003	Sukesh Sandhu	303.596US2	6187
21186	7590	07/05/2006	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			NGUYEN, THANH T	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/716,765	SANDHU ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 24 April 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-41 is/are pending in the application.
  - 4a) Of the above claim(s) 4-6 and 10-12 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-3,7-9 and 13-41 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date: _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1-3, 7-9 and 13-41 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-8, 13, 16, 18-20, 25, 27-28, 31-32, 34-41 are rejected 35 U.S.C. 103(a) as being unpatentable over Yoon et al. (U.S. Patent No. 5,688,724) in view of Wurster et al. (U.S. Patent No. 6,828,191).

Referring to figures 1-6, Yoon et al. teaches a method of forming a coupling dielectric in a memory cell comprising:

Forming a dielectric stack, wherein forming the dielectric stack includes:

Forming SiO<sub>2</sub> (12) on a substrate (10) to the depth of about 30 angstroms (see col. 4, lines 8-10) by thermally grown (see col. 4, 1-5, meeting claim 19);

Forming Ta<sub>2</sub>O<sub>5</sub> (14) on the oxide (12), having a crystallization temperature on the oxide to a depth of between about 60 Angstroms and about 100 angstroms (see col. 4, lines 30-32);

Oxidizing the Ta<sub>2</sub>O<sub>5</sub> with rapid thermal process (RTP) at a temperature above the crystallization temperature for Ta<sub>2</sub>O<sub>5</sub> (see col. 4, lines 38-40, meeting claims 1, 7, 15, 18);

Forming a layer of Si<sub>3</sub>N<sub>4</sub> (16, cell nitride) on the layer of Ta<sub>2</sub>O<sub>5</sub> (14) to a depth of between about 40-60 Angstroms (see col. 5, lines 1-4); and.

Forming a layer of SiO<sub>2</sub> (18) on the layer of Si<sub>3</sub>N<sub>4</sub> (16); and

Forming the dielectric stack to a thickness of between 140 and 240 Angstroms (see col. 4, lines 6 to col. 5, lines 12, col. 6, lines 7-8). Noted that layer 12 has the thickness of 10 angstroms, layer 14 has the thickness of 100 angstroms, layer 16 has the thickness of 50 angstroms and layer 18 has the thickness of 40 angstrom. The stack of layers 12/14/16/18 has the total thickness of 200 angstroms.

Regarding to claims 8, 11 forming Ta<sub>2</sub>O<sub>5</sub> on the oxide to a depth of between about 60 Angstroms and about 100 angstroms (see col. 4, lines 30-32).

Regarding to claim 24, 27, the oxide layer formed by CVD process (see col. 4, lines 1-5).

However, the reference does not teach forming the layer of SiO<sub>2</sub> by using water to form a wet gate oxide, the capacitance of the dielectric stack and the specific thickness of the layer. Wurster et al. teaches forming a gate oxide in an oxidizing atmosphere of oxygen or water to form an oxide layer (see col. 6, lines 64-67).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would forming the gate oxide by using water in process of

Yoon et al. as taught by Wurster et al. because forming a gate oxide by using water to protect the device.

It is obvious that since the stack of dielectric layer made from oxide/tantalum oxide/nitride/oxide has the same thickness range as the present invention. It would be obvious that the stack of the dielectric layer would have larger capacitance than the oxide/nitride/oxide.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the thickness range of the oxide layer, the capacitance range of the gate stack, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e. oxide depth about 10-50 angstroms the capacitance greater than 25%), discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - the oxide depth about 10-50 angstroms, oxide depth about 10-50 angstroms the capacitance greater than 25%) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the oxide layer by using any thickness in process of Yoon et al. because determining a optimum range for a layer involves only routine skill in the art.

Claims 1-3, 9, 14, 17, 21-24, 26, 29-30, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon et al. (U.S. Patent No. 5,688,724) in view of Wurster et al. (U.S. Patent No. 6,828,191) as applied to claims 7-8, 13, 16, 18-20, 25, 27-28, 31-32, 34-41 above further in view of Chao et al. (U.S. Patent No. 6,156,600) and Tseng (U.S. patent No. 5,712,208).

Referring to figures 1-6, Yoon et al. teaches a method of forming a coupling dielectric in a memory cell comprising:

Forming  $\text{SiO}_2$  (12) on a substrate (10) to the depth of about 30 angstroms (see col. 4, lines 8-10) by thermally grown (see col. 4, 1-5, meeting claim 19);

Forming  $\text{Ta}_2\text{O}_5$  (14) on the oxide (12), having a crystallization temperature on the oxide to a depth of between about 60 Angstroms and about 100 angstroms (see col. 4, lines 30-32);

Oxidizing the  $\text{Ta}_2\text{O}_5$  with rapid thermal process (RTP) at a temperature above the crystallization temperature for  $\text{Ta}_2\text{O}_5$  (see col. 4, lines 38-40, meeting claims 1, 7, 15, 18);

Forming a layer of  $\text{Si}_3\text{N}_4$  (16, cell nitride) on the layer of  $\text{Ta}_2\text{O}_5$  (14) to a depth of between about 40-60 Angstroms (see col. 5, lines 1-4); and

Forming a layer of  $\text{SiO}_2$  (18, Noted that wetgate oxide is  $\text{SiO}_2$  see instant invention page 6, lines 3-4) on the layer of  $\text{Si}_3\text{N}_4$  (16).

Regarding to claims 8, 11 forming  $\text{Ta}_2\text{O}_5$  on the oxide to a depth of between about 60 Angstroms and about 100 angstroms (see col. 4, lines 30-32).

Regarding to claim 24, 27, the oxide layer formed by CVD process (see col. 4, lines 1-5)

However, the reference does not teach forming an oxide layer by using organic metal CVD, oxidizing the tantalum oxide with RTP in  $\text{N}_2\text{O}$  for about 55-65 seconds, the substrate by

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using n-type substrate, silicon, gallium arsenide, silicon on sapphire, germanium, or amorphous silicon, and the specific thickness range of the layer.

Chao et al. teaches depositing the Tantalum oxide using organic metal (TAETO) by LPCVD process at the thickness of about 70-150 Angstrom, then annealing the layer using RTA process in dinitrogen oxide (N<sub>2</sub>O) at the temperature about 800°C for about 40 sec. to 2 min. (see col. 4, lines 39-46).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would using organic metal (TAETO) to form the tantalum oxide layer in the CVD in process of Yoon et al. as taught by Chao et al. because the process would save time as well as provide a good step coverage.

Tseng et al. teaches in col. 7, lines 21-34, forming a substrate by using either silicon, gallium arsenide, silicon on sapphire, germanium, or amorphous silicon.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would forming a substrate by using either silicon, gallium arsenide, silicon on sapphire, germanium, or amorphous silicon in process of Yoon et al. as taught by Tseng et al. because these materials provide a substrate with low thermal conductivity and high electron mobility.

It is known in the art to form the substrate by using an n-type or p-type to form an NMOS or PMOS transistor.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the substrate by using an n-type in process of

Yoon et al. because forming a substrate by an N-type is known in the art to have an NMOS transistor.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the thickness range of the oxide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e. oxide depth about 10-50 angstroms), discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - the oxide depth about 10-50 angstroms) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the oxide layer by using any thickness in process of Yoon et al. because determining a optimum range for a layer involves only routine skill in the art.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (See MPEP 203.08).



Thanh Nguyen  
Patent Examiner  
Patent Examining Group 2800

TTN